

# New Crosstalk Avoidance Codes Based on a Novel Pattern Classification

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**Abstract**—The crosstalk delay associated with global on-chip interconnects becomes more severe in deep submicron technology, and hence can greatly affect the overall system performance. Based on a delay model proposed by Sotiriadis *et al.*, transition patterns over a bus can be classified according to their delays. Using this classification, crosstalk avoidance codes (CACs) have been proposed to alleviate the crosstalk delays by restricting the transition patterns on a bus. In this paper, we first propose a new classification of transition patterns, and then devise a new family of CACs based on this classification. In comparison to the previous classification, our classification has more classes and the delays of its classes do not overlap, both leading to more accurate control of delays. Our new family of CACs includes some previously proposed codes as well as new codes with reduced delays and improved throughput. Thus, this new family of crosstalk avoidance codes provides a wider variety of tradeoffs between bus delay and efficiency. Finally, since our analytical approach to the classification and CACs treats the technology-dependent parameters as variables, our approach can be easily adapted to a wide variety of technology.

**Index Terms**—Crosstalk avoidance codes, delay, interconnects

## I. INTRODUCTION

RECENT International Technology Roadmap of Semiconductors (ITRS) [1] has shown a troubling trend: while gate delay **decreases** with scaling, global wire delay **increases**. This is because with the process technologies scaling down into deep submicrometer (DSM), the crosstalk delay becomes dominant in global wire delay due to the increasing coupling capacitance between adjacent wires. Hence, the crosstalk delay has become a serious bottleneck of the overall system performance.

The analytical model proposed by Sotiriadis *et al.* [2], [3], a widely used delay model, gives upper bounds on the delay of all wires on a bus. According to [2], [3], the delay of the  $k$ -th wire ( $k \in \{1, 2, \dots, m\}$ ) of an  $m$ -bit bus is given by

$$T_k = \begin{cases} \tau_0[(1 + \lambda)\Delta_1^2 - \lambda\Delta_1\Delta_2], & k = 1 \\ \tau_0[(1 + 2\lambda)\Delta_k^2 - \lambda\Delta_k(\Delta_{k-1} + \Delta_{k+1})], & k \neq 1, m \\ \tau_0[(1 + \lambda)\Delta_m^2 - \lambda\Delta_m\Delta_{m-1}], & k = m, \end{cases} \quad (1)$$

where  $\lambda$  is the ratio of the coupling capacitance between adjacent wires and the ground capacitance,  $\tau_0$  is the propagation delay of a wire free of crosstalk, and  $\Delta_k$  is 1 for  $0 \rightarrow 1$  transition, -1 for  $1 \rightarrow 0$  transition, or 0 for no transition on the  $k$ -th wire. In this model, the delay of the  $k$ -th wire depends

on the transition patterns of at most three wires,  $k-1$ ,  $k$ , and  $k+1$  only. The transition patterns over these three wires can be classified based on Eq. (1) into five classes, denoted by  $Di$  for  $i = 0, 1, 2, 3, 4$ , and the patterns in  $Di$  have a worst-case delay  $(1 + i\lambda)\tau_0$ . This classification enables one to limit the worst-case delay over a bus by restricting the patterns transmitted on the bus. That is, by avoiding all transition patterns in  $Di$  for  $i > i_0$ , one can achieve a worst-case delay of  $(1 + i_0\lambda)\tau_0$  over the bus. Based on this principle, crosstalk avoidance codes (CACs) of different worst-case delays have been proposed (see, for example, [4]–[6]). For example, forbidden overlap codes (FOCs), forbidden transition codes (FTCs), forbidden pattern codes (FPCs), and one lambda codes (OLCs) achieve a worst-case delay of  $(1 + 3\lambda)\tau_0$ ,  $(1 + 2\lambda)\tau_0$ ,  $(1 + 2\lambda)\tau_0$ , and  $(1 + \lambda)\tau_0$ , respectively. Based on Eq. (1), a worst-case delay of  $\tau_0$  can be achieved by assigning two protection wires to each data wire [5]. Other types of CACs, such as those with equalization [7] or two-dimensional CACs [8], have been proposed in the literature. For CACs, since the area and power consumption of their encoder/decoder (CODECs) are all overheads, the complexities of the CODECs are important to the effectiveness of CACs. Thus, efficient CODECs have been proposed for CACs [9]–[11].

The classification of transition patterns based on the model in [2], [3] has two drawbacks. First, the model in [2], [3] has limited accuracy because of its dependence on only three wires: the model overestimates the delays of patterns in  $D1$  through  $D4$ , while it underestimates the delays of patterns in  $D0$ . For this reason, the scheme with a worst-case delay of  $\tau_0$  in [5] is invalid since its actual delay is much greater. Second, the actual delay ranges in some classes overlap with others. This, plus the overestimation of delays for  $D1$  through  $D4$ , implies that the delays of existing CACs are not tightly controlled. These drawbacks motivate us to include more wires and to classify the transition patterns without overlapping delay ranges.

In [12], we have proposed a new analytical five-wire delay model. Two extra neighboring wires are included in the delay model [12], and the delay of the middle wire of five neighboring wires is determined by the transition patterns on all five wires. This five-wire model has better accuracy than the model in [2], [3] for  $Di$  for  $i = 0, 1, 2, 3, 4$  [12]. This work confirms that using more wires leads to improved accuracy.

There are two main contributions in this paper:

- First, we approximate the crosstalk delay in a five-wire model and propose a new classification of transition patterns.
- Second, we propose a family of CACs based on our

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classification.

The work in this paper is different from previous works, including our previous works, in several aspects:

- First, although the delay approximation in this paper is also based on a five-wire model, it is different from that in our previous work [12]. The delay approximation in this paper is carried out by extending the approach in [13] from a three-wire model to a five-wire one.
- Second, our classification of transition patterns is different from that in [2], [3] (based on Eq. (1)), in two aspects. First, our classification has seven classes as opposed to five based on Eq. (1). Second, while the delays of some classes overlap for the classification based on Eq. (1), all classes in our classification have non-overlapping delays. These two key differences allow us to have a more accurate control of delays for transition patterns.
- Our new family of CACs is also different from previously proposed CACs, all of which are based on the classification in [2], [3] (based on Eq. (1)). While some codes in this new family are shown to be the same as existing CACs, OLCs, FPCs, and FOCs, this family also includes new codes that achieve smaller worst-case delays and improved throughputs than OLCs, which have the smallest worst-case delays among all existing CACs.

The rest of the paper is organized as follows. In Section II, we first propose our classification and compare it with that in [2], [3]. We then present our new family of CACs in Section III and compare their performance with existing CACs in Section IV. Some concluding remarks are provided in Section V.

## II. INTERCONNECT DELAYS AND CLASSIFICATION

### A. Interconnect Modeling

Since the functionality and performance in DSM technology are greatly affected by the parasitics, distributed RC models are widely employed to analyze on-chip interconnects. In this paper, we consider the distributed RC model of five wires shown in Fig. 1, where  $V_i(x, t)$  denotes the transient signal at time  $t$  and position  $x$  ( $0 \leq x \leq L$ ) over wire  $i$  for  $i \in \{1, 2, 3, 4, 5\}$ ,  $r$  and  $c$  denote the resistance and ground capacitance per unit length, respectively. Also,  $\lambda c$  denotes the coupling capacitance per unit length between two adjacent wires. The value of  $\lambda$  depends on many factors, such as the metal layer in which we route the bus, the wire width, the spacing between adjacent wires, and the distance to the ground layer. We consider a uniformly distributed bus with the same parameters  $r$ ,  $c$ , and  $\lambda$  for all the wires.

### B. Derivation of Closed-form Expressions

When determining the delay of a wire, the model in [2], [3] considers only the effects of either **one** or **two** neighboring wires (cf. Eq. (1)). To address the drawbacks of the model in [2], [3] described above, additional neighboring wires need to be accounted for. In our delay derivation below, whenever possible we consider **four** neighboring wires of a wire, two

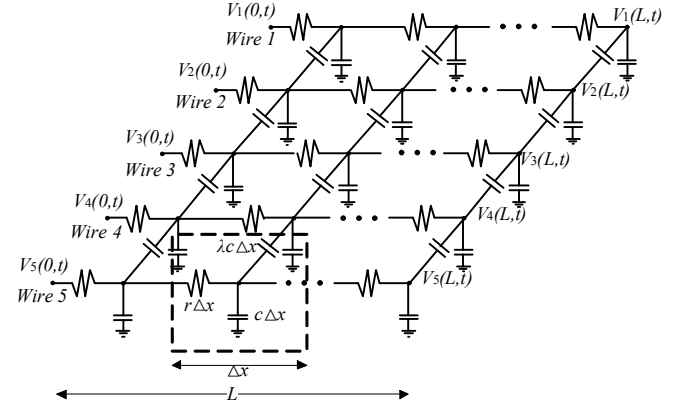


Fig. 1. A distributed RC model for five wires.

neighboring wires on each side, to determine its delay. To approximate the delay of a side wire (wires 1, 2,  $n-1$  or  $n$ ) of an  $n$ -wire bus, **three** neighboring wires are considered. This is because the side wires are affected by fewer neighboring wires. This scheme is similar to the model in [2], [3] and appears to work well. We focus on the 50% delay, which is defined as the time required for the unit step response to reach 50% of its final value.

In [13], the crosstalk of two coupled lines was described by partial differential equations (PDEs), and a technique for decoupling these highly coupled PDEs was introduced by using eigenvalues and corresponding eigenvectors. In our work, we extend this approach from a three-wire model to a five-wire one. Specifically, we first use the technique in [13] to decouple the PDEs that describe the crosstalk of four coupled wires, then solve these independent PDEs for closed-form expressions, and finally approximate the delays of each wire.

The PDEs characterizing five wires with length  $L$  are given by:

$$\frac{\partial^2}{\partial x^2} \mathbf{V}(x, t) = \mathbf{RC} \frac{\partial}{\partial t} \mathbf{V}(x, t), \quad (2)$$

where  $\mathbf{R} = \text{diag}\{r \ r \ r \ r \ r\}$ ,  $\mathbf{V}(x, t) = [V_1(x, t) \ V_2(x, t) \ V_3(x, t) \ V_4(x, t) \ V_5(x, t)]^T$ , and

$$\mathbf{C} = c \begin{bmatrix} 1+\lambda & -\lambda & 0 & 0 & 0 \\ -\lambda & 1+2\lambda & -\lambda & 0 & 0 \\ 0 & -\lambda & 1+2\lambda & -\lambda & 0 \\ 0 & 0 & -\lambda & 1+2\lambda & -\lambda \\ 0 & 0 & 0 & -\lambda & 1+\lambda \end{bmatrix}.$$

The eigenvalues of  $\mathbf{C}/c$  are given by  $p_1 = 1$ ,  $p_2 = 1 + \frac{5+\sqrt{5}}{2}\lambda$ ,  $p_3 = 1 + \frac{5-\sqrt{5}}{2}\lambda$ ,  $p_4 = 1 + \frac{3+\sqrt{5}}{2}\lambda$ , and  $p_5 = 1 + \frac{3-\sqrt{5}}{2}\lambda$ . Their corresponding eigenvectors  $\mathbf{e}_i$ 's are given by  $\mathbf{e}_1 = [1 \ 1 \ 1 \ 1 \ 1]^T$ ,  $\mathbf{e}_2 = [\frac{\sqrt{5}-1}{4} \ -\frac{1+\sqrt{5}}{4} \ 1 \ -\frac{1+\sqrt{5}}{4} \ \frac{\sqrt{5}-1}{4}]^T$ ,  $\mathbf{e}_3 = [\frac{-\sqrt{5}+1}{4} \ \frac{\sqrt{5}-1}{4} \ 1 \ \frac{\sqrt{5}-1}{4} \ -\frac{\sqrt{5}+1}{4}]^T$ ,  $\mathbf{e}_4 = [-1 \ \frac{\sqrt{5}+1}{2} \ 0 \ -\frac{\sqrt{5}+1}{2} \ 1]^T$ , and  $\mathbf{e}_5 = [-1 \ -\frac{\sqrt{5}-1}{2} \ 0 \ \frac{\sqrt{5}-1}{2} \ 1]^T$ , respectively.

With a technique for decoupling partial differential equations similar to [13], Eq. (2) is transformed into

$$\frac{\partial^2}{\partial x^2} U_i(x, t) = r c p_i \frac{\partial}{\partial t} U_i(x, t), \text{ for } i = 1, 2, 3, 4, 5, \quad (3)$$

where  $U_i(x, t) = \mathbf{V}^T(x, t) \mathbf{e}_i$  denotes the transformed signals. The decoupled PDEs in Eq. (3) are independent of each other. Each  $U_i(x, t)$  describes a single wire with a modified capacitance  $c p_i$ . The solution to  $U_i(L, t)$  is given by a series of

the form  $U_i(L, t) = V_{dd} + \sum_{k=0}^{\infty} r_k e^{-\frac{t}{s_k \tau}}$ . As shown in [13], a single-exponent approximation  $V_{dd}(1 + r_0 e^{-\frac{t}{s_0 \tau}})$  is enough for  $t/\tau > 0.1$ , where  $r_0$  and  $s_0$  are the coefficients of the most significant term.

For different transitions, we solve Eq. (3) for  $U_i(x, t)$  and obtain  $V_3(L, t) = \frac{1}{5}[U_1(L, t) + 2U_2(L, t) + 2U_3(L, t)]$ , which is given by a sum of a constant and three exponent terms,  $V_{dd}(1 - c_0 e^{-\frac{t}{a_0 \tau}} - c_1 e^{-\frac{t}{a_1 \tau}} - c_2 e^{-\frac{t}{a_2 \tau}})$ . Then the 50% delay of wire 3 can be evaluated by solving  $V_3(L, t) = 0.5V_{dd}$ .

For side wires, PDEs characterizing four wires with length  $L$  are given by:

$$\frac{\partial^2}{\partial x^2} \mathbf{V}(x, t) = \mathbf{RC} \frac{\partial}{\partial t} \mathbf{V}(x, t), \quad (4)$$

where  $\mathbf{R} = \text{diag}\{r \ r \ r \ r\}$ ,  $\mathbf{V}(x, t) = [V_1(x, t) \ V_2(x, t) \ V_3(x, t) \ V_4(x, t)]^T$ , and  $\mathbf{C} = c \begin{bmatrix} 1+\lambda & -\lambda & 0 & 0 \\ -\lambda & 1+2\lambda & -\lambda & 0 \\ 0 & -\lambda & 1+2\lambda & -\lambda \\ 0 & 0 & -\lambda & 1+\lambda \end{bmatrix}$ .

The eigenvalues of  $\mathbf{C}/c$  are given by  $p_1 = 1$ ,  $p_2 = 1 + (2 - \sqrt{2})\lambda$ ,  $p_3 = 1 + 2\lambda$ , and  $p_4 = 1 + (2 + \sqrt{2})\lambda$ . Their corresponding eigenvectors  $\mathbf{e}_i$ 's are given by  $\mathbf{e}_1 = [1 \ 1 \ 1 \ 1]^T$ ,  $\mathbf{e}_2 = [-1 \ (1 - \sqrt{2}) \ -(1 - \sqrt{2}) \ 1]^T$ ,  $\mathbf{e}_3 = [1 \ -1 \ -1 \ 1]^T$ , and  $\mathbf{e}_4 = [-1 \ (1 + \sqrt{2}) \ -(1 + \sqrt{2}) \ 1]^T$ , respectively.

By decoupling the PDEs in Eq. (4), we have

$$\frac{\partial^2}{\partial x^2} U_i(x, t) = r c p_i \frac{\partial}{\partial t} U_i(x, t), \text{ for } i = 1, 2, 3, 4, \quad (5)$$

The expressions of wires 1 and 2 are given by  $V_1(L, t) = \frac{1}{4}U_1(L, t) - \frac{2+\sqrt{2}}{8}U_2(L, t) + \frac{1}{4}U_3(L, t) - \frac{2-\sqrt{2}}{8}U_4(L, t)$  and  $V_2(L, t) = \frac{1}{4}U_1(L, t) - \frac{\sqrt{2}}{8}U_2(L, t) - \frac{1}{4}U_3(L, t) + \frac{\sqrt{2}}{8}U_4(L, t)$ , respectively. Then the 50% delays of wires 1 and 2 can be evaluated by solving  $V_i(L, t) = 0.5V_{dd}$  for  $i = 1, 2$ .

### C. Pattern Classification

First, we consider the classification of transition patterns over five wires with respect to the delay of the middle wire (wire 3). In this paper, we use “ $\uparrow$ ” to denote a transition from 0 to the supply voltage  $V_{dd}$  (normalized to 1), “-” no transition, and “ $\downarrow$ ” a transition from  $V_{dd}$  to 0. We first focus on patterns with a  $\uparrow$  transition on wire 3 in a five-wire bus and derive  $V_3(L, t)$  for each pattern as described in Sec. II-B. There are  $3^4 = 81$  different transition patterns, which can be partitioned into 25 subclasses according to the expressions of the output signals on wire 3: All transition patterns in each subclass have the same expression  $V_3(L, t)$ . The expressions of all 25 subclasses are shown in Tab. I. Then the expressions  $V_3(L, t)$  of all patterns in the 25 subclasses are evaluated for their 50% delays. By grouping subclasses with close delays into one class, we can divide the 81 transition patterns into seven classes  $C_i$  for  $i = 0, 1, \dots, 6$  shown in Tab. I. For all 25 subclasses, simulated delays are also provided in Tab. I. For all seven classes, the difference between evaluated delay and simulated delay in Tab. I is small.

All evaluations and simulations are based on a freePDK 45nm CMOS technology with 10 metal layers [14]. We assume that the top two metal layers, layers 9 and 10, are used for routing global interconnects, and that metal layer 8 is used as

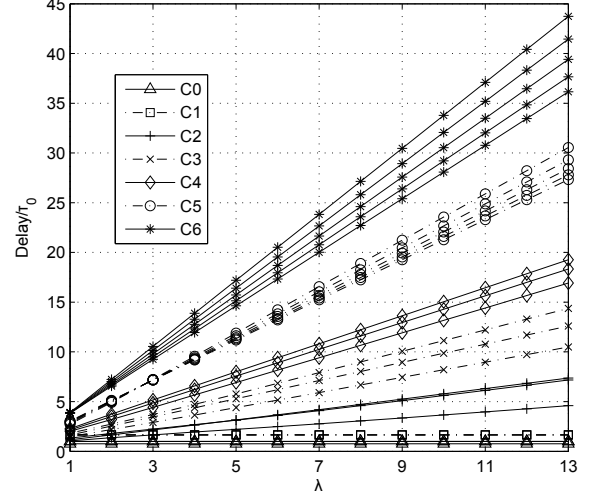


Fig. 2. Delays of the middle wire for all patterns with respect to  $\lambda$  in a five-wire bus ( $\tau_0 = 1.42\text{ps}$ ).

the ground layer. An interconnect model in [15] is used for parasitic extraction. For a 5mm bus in the top metal layer, the key parasitics, resistance, ground capacitance, and coupling capacitance, are given by  $R = 68.75\Omega$ ,  $C_{gnd} = 41.32\text{fF}$ , and  $C_{couple} = 505.68\text{fF}$ , respectively. The bus is modeled by a distributed RC model as shown in Fig. 1 with 100 segments. The two important parameters used in our delay approximation are  $\tau_0 = 0.5RC_{gnd} = 1.42\text{ps}$  and  $\lambda = C_{couple}/C_{gnd} = 12.24$ . Since the crosstalk delay on the bus constitutes a major part of the whole delay, the delays introduced by buffers are ignored. We assume that ideal step signals are applied on the bus directly. The closed-form expressions are evaluated for 50% delays via MATLAB and the simulation is done by HSPICE.

From Tab. I, it can be easily verified that  $C5$  and  $C6$  are the same as  $D3$  and  $D4$  in [2], [3], respectively. That is, the middle three wires of the transition patterns in  $C5$  ( $C6$ , respectively) constitute  $D3$  ( $D4$ , respectively). The transition patterns in  $D0$ ,  $D1$ , and  $D2$  are divided into five classes  $C0$ — $C4$  in our classification with following relations,  $C4 \subset D2$ ,  $C3 \subset D1 \cup D2$ ,  $C2 \subset D0 \cup D1$ ,  $C1 \subset D0 \cup D1 \cup D2$ , and  $C0 \subset D0 \cup D1$ .

Note that the coefficients  $c_i$  for  $i = 0, 1, 2$  of the expression of wire 3 are independent of technology and determined by different patterns. For a given pattern, the coefficients  $c_i$  are fixed and the delay is a function of  $\tau_0$  and  $\lambda$ . Since the ratio  $t/\tau_0$  appears in the exponent term, varying  $\tau_0$  would scale delays in all classes. Thus, the classification does not depend on  $\tau_0$ . The coupling factor  $\lambda$  could affect the delay differently. In the following, we verify our classification for technology with different coupling factor,  $\lambda = 1, 2, \dots, 13$ , and show the results in Fig. 2. Different classes are denoted by different line styles. Each class contains multiple lines, which represents a subclass. Patterns in each subclass have the same delay. For  $\lambda \geq 3$ , the ranges of delays in all classes do not overlap. Also, the delay in each subclass increases linearly with  $\lambda$ . This implies that our classification is valid provided that the coupling factor  $\lambda$  is at least 3.

TABLE I

CLOSED-FORM EXPRESSIONS FOR THE OUTPUT SIGNALS ON WIRE 3 IN A FIVE-WIRE BUS WITH EVALUATED AND SIMULATED 50% DELAYS ( $\tau_0 = 1.42$  ps,  $\tau = \frac{8}{\pi^2} \tau_0$ ,  $\lambda = 12.24$ ,  $a_0 = 1$ ,  $a_1 = 1 + \frac{5-\sqrt{5}}{2} \lambda$ , AND  $a_2 = 1 + \frac{5+\sqrt{5}}{2} \lambda$  FOR ALL CLASSES).

Class $i$	Patterns	Closed-form expression for output signal on wire 3			Evaluated delays (ps)	Sim. delay (ps)
		$V_{dd}(1 - c_0 e^{-\frac{t}{a_0 \tau}} - c_1 e^{-\frac{t}{a_1 \tau}} - c_2 e^{-\frac{t}{a_2 \tau}})$				
		$c_0$	$c_1$	$c_2$		
0	$\uparrow\uparrow\uparrow\uparrow$	$\frac{4}{\pi}$	0	0	1.08	1.18
	$-\uparrow\uparrow\uparrow, \uparrow\uparrow\uparrow-$	$\frac{16}{5\pi}$	$\frac{2(1+\sqrt{5})}{5\pi}$	$\frac{2(1-\sqrt{5})}{5\pi}$	<b>1.41</b>	<b>1.50</b>
	$\uparrow-\uparrow\uparrow, \uparrow\uparrow-\uparrow$	$\frac{16}{5\pi}$	$\frac{2(1-\sqrt{5})}{5\pi}$	$\frac{2(1+\sqrt{5})}{5\pi}$	<b>1.41</b>	<b>1.50</b>
1	$-\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow, \uparrow\uparrow\uparrow\downarrow$	$\frac{12}{5\pi}$	$\frac{4(1+\sqrt{5})}{5\pi}$	$\frac{4(1-\sqrt{5})}{5\pi}$	<b>2.35</b>	2.40
	$- -\uparrow\uparrow\uparrow, \uparrow\uparrow\uparrow- -, -\uparrow\uparrow\uparrow, \uparrow-\uparrow\uparrow-$	$\frac{12}{5\pi}$	$\frac{4}{5\pi}$	$\frac{4}{5\pi}$	<b>2.35</b>	2.40
	$\uparrow-\uparrow\uparrow, \uparrow\uparrow\uparrow\downarrow, \uparrow\downarrow\uparrow\uparrow$	$\frac{12}{5\pi}$	$\frac{4(1-\sqrt{5})}{5\pi}$	$\frac{4(1+\sqrt{5})}{5\pi}$	<b>2.35</b>	<b>2.45</b>
2	$-\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow-$	$\frac{8}{5\pi}$	$\frac{6(1+\sqrt{5})}{5\pi}$	$\frac{6(1-\sqrt{5})}{5\pi}$	6.17	6.84
	$- -\uparrow\uparrow\uparrow, -\uparrow\uparrow\uparrow- -, \downarrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow-$	$\frac{8}{5\pi}$	$\frac{2(3+\sqrt{5})}{5\pi}$	$\frac{2(3-\sqrt{5})}{5\pi}$	9.62	9.21
	$\uparrow-\uparrow\uparrow\downarrow, \uparrow\uparrow\uparrow\downarrow$	$\frac{4}{5\pi}$	$\frac{8(1+\sqrt{5})}{5\pi}$	$\frac{8(1-\sqrt{5})}{5\pi}$	<b>9.90</b>	<b>10.70</b>
3	$- -\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow- -, -\uparrow\uparrow\uparrow\downarrow, \downarrow-\uparrow\uparrow\uparrow-$	$\frac{4}{5\pi}$	$\frac{4(2+\sqrt{5})}{5\pi}$	$\frac{4(2-\sqrt{5})}{5\pi}$	14.07	14.22
	$\downarrow-\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\downarrow$	0	$\frac{2(5+3\sqrt{5})}{5\pi}$	$\frac{2(5-3\sqrt{5})}{5\pi}$	16.91	17.18
	$- -\uparrow\uparrow\uparrow\downarrow, \uparrow\uparrow\uparrow\uparrow- -, -\uparrow\uparrow\uparrow\downarrow\uparrow, \uparrow\uparrow\uparrow\uparrow\downarrow-, -\downarrow\uparrow\uparrow\uparrow, \uparrow\downarrow\uparrow\uparrow-$	$\frac{8}{5\pi}$	$\frac{2(3-\sqrt{5})}{5\pi}$	$\frac{2(3+\sqrt{5})}{5\pi}$	<b>19.24</b>	<b>18.47</b>
4	$- -\uparrow\uparrow\uparrow- -, \uparrow\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\uparrow, -\uparrow\uparrow\uparrow\downarrow, \uparrow\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\uparrow\uparrow, -\downarrow\uparrow\uparrow\uparrow, \uparrow\downarrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow\uparrow\uparrow$	$\frac{4}{5\pi}$	$\frac{8}{5\pi}$	$\frac{8}{5\pi}$	22.67	22.60
	$- -\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\uparrow-, -\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\uparrow\downarrow, -\downarrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow\uparrow\downarrow, -\downarrow\uparrow\uparrow\uparrow\uparrow, \downarrow\uparrow\uparrow\uparrow\uparrow\downarrow$	0	$\frac{2(5+\sqrt{5})}{5\pi}$	$\frac{2(5-\sqrt{5})}{5\pi}$	24.58	24.68
	$\downarrow\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow\downarrow$	$-\frac{4}{5\pi}$	$\frac{4(3+\sqrt{5})}{5\pi}$	$\frac{4(3-\sqrt{5})}{5\pi}$	<b>25.84</b>	<b>26.03</b>
5	$\downarrow\downarrow\uparrow\downarrow, \downarrow\uparrow\uparrow\downarrow$	$-\frac{8}{5\pi}$	$\frac{2(7+\sqrt{5})}{5\pi}$	$\frac{2(7-\sqrt{5})}{5\pi}$	36.63	36.91
	$- -\uparrow\uparrow\downarrow, \downarrow\uparrow\uparrow\uparrow- -, -\downarrow\uparrow\uparrow\downarrow, \downarrow-\uparrow\uparrow\downarrow$	$-\frac{4}{5\pi}$	$\frac{12}{5\pi}$	$\frac{12}{5\pi}$	37.24	37.52
	$- -\uparrow\uparrow\downarrow, -\downarrow\uparrow\uparrow- -, \uparrow\uparrow\uparrow\downarrow, \uparrow\downarrow\uparrow\downarrow, \downarrow\uparrow\downarrow\uparrow, \downarrow\uparrow\downarrow\uparrow$	0	$\frac{2(5-\sqrt{5})}{5\pi}$	$\frac{2(5+\sqrt{5})}{5\pi}$	38.07	38.35
	$- -\uparrow\uparrow\downarrow, \uparrow\downarrow\uparrow\uparrow- -, -\downarrow\uparrow\uparrow\uparrow, \uparrow-\uparrow\uparrow\downarrow$	$\frac{4}{5\pi}$	$\frac{4(2-\sqrt{5})}{5\pi}$	$\frac{4(2+\sqrt{5})}{5\pi}$	39.22	39.47
	$\uparrow-\uparrow\downarrow\uparrow, \uparrow\downarrow\uparrow\uparrow$	$\frac{8}{5\pi}$	$\frac{6(1-\sqrt{5})}{5\pi}$	$\frac{6(1+\sqrt{5})}{5\pi}$	<b>40.87</b>	<b>41.11</b>
6	$\downarrow\downarrow\uparrow\downarrow\downarrow$	$-\frac{12}{5\pi}$	$\frac{16}{5\pi}$	$\frac{16}{5\pi}$	48.43	48.85
	$\downarrow\downarrow\uparrow\downarrow-, -\downarrow\uparrow\downarrow\downarrow$	$-\frac{8}{5\pi}$	$\frac{2(7-\sqrt{5})}{5\pi}$	$\frac{2(7+\sqrt{5})}{5\pi}$	50.43	50.86
	$-\downarrow\uparrow\downarrow, \uparrow\downarrow\uparrow\downarrow, \downarrow\downarrow\uparrow\downarrow\uparrow$	$-\frac{4}{5\pi}$	$\frac{4(3-\sqrt{5})}{5\pi}$	$\frac{4(3+\sqrt{5})}{5\pi}$	52.78	53.25
	$\uparrow\downarrow\uparrow\downarrow-, -\downarrow\uparrow\downarrow\uparrow$	0	$\frac{4(5-3\sqrt{5})}{5\pi}$	$\frac{4(5+3\sqrt{5})}{5\pi}$	55.48	55.97
	$\uparrow\downarrow\uparrow\downarrow\uparrow$	$\frac{4}{5\pi}$	$\frac{8(1-\sqrt{5})}{5\pi}$	$\frac{8(1+\sqrt{5})}{5\pi}$	<b>58.52</b>	<b>59.04</b>

Then, we consider the classification of transition patterns over four wires with respect to the delays of the side wires. We classify patterns by considering the worst-case delays of wires 1 and 2, respectively. Note that the classification with respect to the delays of wires 4 and 5 would be the same by symmetry. We first focus on patterns with a  $\uparrow$  transition on wire 2 in a four-wire bus. There are  $3^3 = 27$  different transition patterns. As described in Sec. II-B, we first derive the expressions  $V_2(L, t)$  of these 27 patterns shown in Tab. II. By evaluating these patterns for their 50% delays, we group patterns with close delays into one class, and form 5 classes  $jC$  for  $j = 0, 1, 2, 3, 4$  as shown in Tab. II. Then, we focus on patterns with a  $\uparrow$  transition on wire 1. There are  $3^3 = 27$  different transition patterns. As described in Sec. II-B, we first derive the expressions  $V_1(L, t)$  of these 27 patterns shown in Tab. III. By evaluating these patterns for their 50% delays, we group patterns with close delays into one class, and form 3 classes  $jC$  for  $j = 0, 1, 2$  as shown in Tab. III. When both wires 1 and 2 have transitions, the delay on wire 2 is larger

than that of wire 1, which can be verified from Tabs. II and III. In this case, we focus on the delay of wire 2. When only wire 1 has transition, we focus on the delay of wire 1. The difference between evaluated delay and simulated delay is small as shown in Tabs. II and III with one exception (the pattern  $\uparrow\uparrow\uparrow\downarrow$  in 1C in Tab. II), which doesn't change our classification.

From Tabs. II and III, the classes 3C and 4C of our classification are exactly the same as D3 and D4 in [2], [3], respectively. The class 1C and 2C of our classification are subsets of D1 and D2 in [2], [3], respectively. The class 0C is a subset of  $D0 \cup D1$  in [2], [3].

Similar to the classification of middle wires, we conclude that the classification on side wires does not depend on  $\tau_0$ . To verify our classification for technology with different coupling effects, we consider coupling factor  $\lambda = 1, 2, \dots, 13$ , and show the results in Fig. 3. Each class contains multiple lines, each of which represents a pattern in Tabs. II and III. For  $\lambda \geq 1$ , the ranges of delays in all classes do not overlap. Also, the delay in each subclass increases linearly with  $\lambda$ . This

TABLE II

CLOSED-FORM EXPRESSIONS FOR THE OUTPUT SIGNALS ON WIRE 2 IN A FOUR-WIRE BUS WITH EVALUATED AND SIMULATED 50% DELAYS ( $\tau_0 = 1.42$  ps,  $\tau = \frac{8}{\pi^2}\tau_0$ ,  $\lambda = 12.24$ ,  $a_0 = 1$ ,  $a_1 = 1 + (2 - \sqrt{2})\lambda$ ,  $a_2 = 1 + 2\lambda$ , AND  $a_3 = 1 + (2 + \sqrt{2})\lambda$  FOR ALL CLASSES).

$jC$	Patterns	Closed-form expression for the output signal on wire 2				Evaluated delays (ps)	Sim. delay (ps)
		$V_{dd}(1 - c_0 e^{-\frac{t}{a_0\tau}} - c_1 e^{-\frac{t}{a_1\tau}} - c_2 e^{-\frac{t}{a_2\tau}} - c_3 e^{-\frac{t}{a_3\tau}})$					
		$c_0$	$c_1$	$c_2$	$c_3$		
0	↑↑↑↑	$\frac{4}{\pi}$	0	0	0	1.08	1.18
	↑↑↑-	$\frac{3}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	<b>1.55</b>	1.61
	↑↑-↑	$\frac{3}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$-\frac{2+\sqrt{2}}{2\pi}$	<b>1.55</b>	1.62
	-↑↑↑	$\frac{3}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	<b>1.55</b>	<b>1.64</b>
1	↑↑↑↓	$\frac{2}{\pi}$	$\frac{\sqrt{2}}{\pi}$	$\frac{2}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	3.33	3.22
	↑↑- -	$\frac{2}{\pi}$	$\frac{1}{\pi}$	0	$\frac{1}{\pi}$	4.54	3.48
	-↑↑-	$\frac{2}{\pi}$	0	$\frac{2}{\pi}$	0	7.21	5.15
	↑↑-↓	$\frac{1}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	9.70	9.38
	↑↑↓↑	$\frac{2}{\pi}$	0	$\frac{2-\sqrt{2}}{2\pi}$	$-\frac{2}{\pi}$	9.98	3.92
	-↑↑↓	$\frac{1}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	<b>12.89</b>	<b>13.03</b>
2	↑↑↓-	$\frac{1}{\pi}$	$\frac{4-\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$\frac{4+\sqrt{2}}{2\pi}$	17.02	16.05
	-↑↑↑	$\frac{2}{\pi}$	$\frac{1-\sqrt{2}}{2\pi}$	0	$\frac{1+\sqrt{2}}{2\pi}$	19.67	18.79
	↑↑↓↓	0	$\frac{2}{\pi}$	0	$\frac{2}{\pi}$	20.05	19.85
	-↑- -	$\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	22.59	22.48
	-↑-↓	0	$\frac{1}{\pi}$	$\frac{2}{\pi}$	$\frac{1}{\pi}$	24.12	24.22
	↓↑↑↑	$\frac{2}{\pi}$	$-\frac{\sqrt{2}}{\pi}$	$\frac{2}{\pi}$	$\frac{\sqrt{2}}{\pi}$	26.02	26.06
	↓↑↑-	$\frac{1}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	26.89	27.06
	↓↑↑↓	0	0	$\frac{4}{\pi}$	0	<b>27.45</b>	<b>27.68</b>
3	-↑↓↓	$-\frac{1}{\pi}$	$\frac{4-\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{4+\sqrt{2}}{2\pi}$	37.44	37.74
	-↑↓-	0	$\frac{2-\sqrt{2}}{2\pi}$	0	$\frac{2+\sqrt{2}}{2\pi}$	38.61	38.89
	↓↑-↓	$-\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	39.06	39.40
	-↑↓↑	$\frac{1}{\pi}$	$\frac{4-\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$\frac{4+\sqrt{2}}{2\pi}$	40.12	40.39
	↓↑- -	0	$\frac{1-\sqrt{2}}{2\pi}$	$\frac{2}{\pi}$	$\frac{1+\sqrt{2}}{2\pi}$	40.21	40.55
	↓↑↑↑	$\frac{1}{\pi}$	$\frac{2-3\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2+3\sqrt{2}}{2\pi}$	<b>41.63</b>	<b>41.98</b>
4	↓↑↓↓	$-\frac{2}{\pi}$	$\frac{2-\sqrt{2}}{\pi}$	$\frac{2}{\pi}$	$\frac{2+\sqrt{2}}{\pi}$	50.92	51.36
	↓↑↓-	$-\frac{1}{\pi}$	$\frac{4-3\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{4+3\sqrt{2}}{2\pi}$	52.99	53.44
	↓↑↓↑	0	$\frac{2-2\sqrt{2}}{\pi}$	0	$\frac{2+2\sqrt{2}}{\pi}$	<b>55.28</b>	<b>55.79</b>

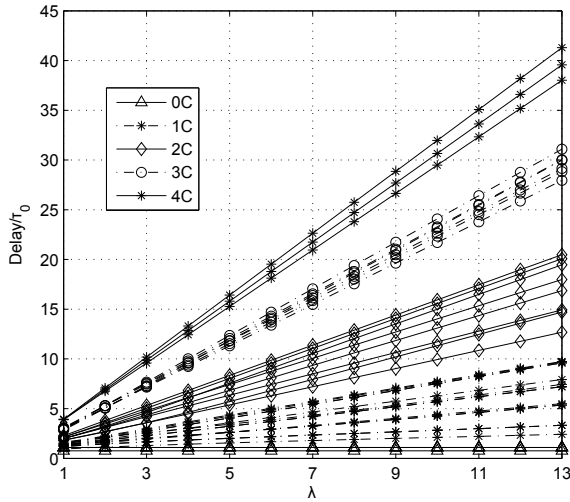


Fig. 3. Delays of side wires for all patterns with respect to  $\lambda$  in a four-wire bus ( $\tau_0 = 1.42$ ps).

implies that our classification on side wires is valid provided that the coupling factor  $\lambda$  is at least 1.

In addition to being a finer classification, the new classification has no overlapping delays among different classes. Fig. 4 compares the simulated delays of different classes based on the classification in [2], [3] and our new classification. In Fig. 4, the grey bars identify the minimum and maximum simulated delays in every class. Note that only two extremes are important, and not all delay values in the grey bars are achievable by some transition patterns. In Fig. 4(a), the thick line segments denote the upper bounds for delay of each class based on Eq. (1). The upper bounds by the model in [2], [3] overestimate the delays of  $D1$  through  $D4$  and underestimate the delay of  $D0$ . As shown in Fig. 4(a), the actual delays in  $D0$ ,  $D1$ , and  $D2$  overlap with each other. Some patterns with smaller delays have potential to transmit information at a higher speed, but are categorized into a class with a larger delay bound. Thus, the classification by the model in [2], [3] does not result in effective crosstalk avoidance codes. In contrast, the delays of different classes in our new classification do not overlap as shown in Fig. 4(b), 4(c), and 4(d). By classifying patterns this way, we have a more accurate

TABLE III

CLOSED-FORM EXPRESSIONS FOR THE OUTPUT SIGNALS ON WIRE 1 IN A FOUR-WIRE BUS WITH EVALUATED AND SIMULATED 50% DELAYS ( $\tau_0 = 1.42$  ps,  $\tau = \frac{8}{\pi^2}\tau_0$ ,  $\lambda = 12.24$ ,  $a_0 = 1$ ,  $a_1 = 1 + (2 - \sqrt{2})\lambda$ ,  $a_2 = 1 + 2\lambda$ , AND  $a_3 = 1 + (2 + \sqrt{2})\lambda$  FOR ALL CLASSES).

$jC$	Patterns	Closed-form expression for the output signal on wire 1				Evaluated delays (ps)	Sim. delay (ps)
		$V_{dd}(1 - c_0e^{-\frac{t}{a_0\tau}} - c_1e^{-\frac{t}{a_1\tau}} - c_2e^{-\frac{t}{a_2\tau}} - c_3e^{-\frac{t}{a_3\tau}})$					
		$c_0$	$c_1$	$c_2$	$c_3$		
0	↑↑↑↑	$\frac{4}{\pi}$	0	0	0	1.08	1.18
	↑↑↑-	$\frac{3}{\pi}$	$-\frac{2+\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	<b>1.55</b>	1.59
	↑↑↑-	$\frac{3}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	<b>1.55</b>	1.61
	↑↑↑-	$\frac{3}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	<b>1.55</b>	<b>1.64</b>
1	↑↑↑↓	$\frac{2}{\pi}$	$\frac{2+\sqrt{2}}{\pi}$	$-\frac{2}{\pi}$	$\frac{2-\sqrt{2}}{\pi}$	2.50	2.70
	↑↑- -	$\frac{2}{\pi}$	$\frac{1+\sqrt{2}}{\pi}$	0	$\frac{1-\sqrt{2}}{\pi}$	2.83	2.90
	↑↑↓↑	$\frac{2}{\pi}$	$\frac{\sqrt{2}}{\pi}$	$\frac{2}{\pi}$	$-\frac{\sqrt{2}}{\pi}$	3.33	3.20
	↑↑↓↓	$\frac{1}{\pi}$	$\frac{4+3\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$\frac{4-3\sqrt{2}}{2\pi}$	4.65	4.99
	↑↑↑↓	$\frac{2}{\pi}$	$\frac{1}{2\pi}$	0	$\frac{1}{2\pi}$	4.54	3.49
	↑↑↓↑	$\frac{1}{\pi}$	$\frac{2+3\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2-3\sqrt{2}}{2\pi}$	5.53	5.88
	↑↑↓↓	0	$\frac{2+2\sqrt{2}}{\pi}$	0	$\frac{2-2\sqrt{2}}{\pi}$	7.03	7.39
	↑↑↑↑	$\frac{2}{\pi}$	0	$\frac{2}{\pi}$	0	7.21	5.15
	↑↑↓↓	$\frac{1}{\pi}$	$\frac{4+\sqrt{2}}{2\pi}$	$-\frac{1}{\pi}$	$\frac{4-\sqrt{2}}{2\pi}$	7.41	6.89
	↑↑--	$\frac{1}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	9.70	9.35
	↑↑↓↑	0	$\frac{2+\sqrt{2}}{\pi}$	0	$\frac{2-\sqrt{2}}{\pi}$	10.68	10.54
	↑↑↓↓	$\frac{1}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	12.89	13.03
	↑↑↓↑	0	$\frac{2+2\sqrt{2}}{2\pi}$	$\frac{2}{\pi}$	$\frac{2-2\sqrt{2}}{2\pi}$	13.03	13.14
	↑↑↓↓	$-\frac{1}{\pi}$	$\frac{4+3\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{4-3\sqrt{2}}{2\pi}$	<b>13.11</b>	<b>13.21</b>
2	↑↓↑↓	0	$\frac{2}{\pi}$	0	$\frac{2}{\pi}$	20.05	19.85
	↑↓↓↓	$-\frac{1}{\pi}$	$\frac{4+\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{4-\sqrt{2}}{2\pi}$	21.86	21.91
	↑↓↑↑	$\frac{1}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	$\frac{1}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	22.59	22.48
	↑↓↓↓	$-\frac{2}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	$\frac{2}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	23.10	23.23
	↑↓- -	0	$\frac{1}{\pi}$	$\frac{2}{\pi}$	$\frac{1}{\pi}$	24.12	24.22
	↑↓↓↓	$-\frac{1}{\pi}$	$\frac{2+\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$\frac{2-\sqrt{2}}{2\pi}$	25.10	25.30
	↑↓↑↑	$\frac{2}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	$\frac{2}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	26.02	26.06
	↑↓↑↑	$\frac{1}{\pi}$	$-\frac{\sqrt{2}}{2\pi}$	$\frac{3}{\pi}$	$\frac{\sqrt{2}}{2\pi}$	26.89	27.06
	↑↓↑↑	0	0	$\frac{1}{\pi}$	0	<b>27.45</b>	<b>27.68</b>

control of delays for transition patterns.

### III. NEW MEMORYLESS CROSSTALK AVOIDANCE CODES

#### A. Previous CAC Design

CACs reduce the crosstalk delay for on-chip global interconnects by encoding a  $k$ -bit data word ( $x_1x_2 \cdots x_k$ ) into an  $n$ -bit ( $n > k$ ) codeword ( $c_1c_2 \cdots c_n$ ). Two kinds of CACs, CACs with memory and memoryless CACs, have been investigated in the literature. CACs with memory, as shown in Fig. 5(a), need to store all codebooks corresponding to different codewords ( $c_1c_2 \cdots c_n$ ), since the encoding depends on the data word ( $x_1x_2 \cdots x_k$ ) as well as the preceding codeword. In contrast, memoryless CACs, as shown in Fig. 5(b), require a single codebook to generate codewords for transmission, because the encoding depends on the data word only. Hence, memoryless CACs are simpler to implement than CACs with memory. We focus on memoryless CACs in this paper.

The codebook of a memoryless CAC satisfies the property that each codeword must be able to transition to every other codeword in the codebook with a delay less than the requirement. Most memoryless CACs in the literature are based on

the model in [2], [3]. The key idea is to eliminate undesirable patterns for transmission. Existing memoryless CACs include OLCs, FPCs, FTCs, and FOCs [4]–[6], [16], which achieve a worst-case delay of  $(1 + \lambda)\tau_0$ ,  $(1 + 2\lambda)\tau_0$ ,  $(1 + 2\lambda)\tau_0$ , and  $(1 + 3\lambda)\tau_0$ , respectively. As mentioned above, the scheme that was proposed to achieve a worst-case delay of  $\tau_0$  is invalid since the model in [2], [3] underestimates the delays for  $0C$ . Thus, OLCs achieve the smallest worst-case delay  $(1 + \lambda)\tau_0$  among existing CACs.

There exist several methods to obtain a memoryless codebook based on pattern pruning, transition pruning, or recursive construction. The pattern pruning technique is quite straight forward, and gives a codebook with a smaller worst-case delay by eliminating some patterns. For example, FOCs cannot have both 010 and 101 patterns around any bit position, and FPCs are free of 010 and 101 patterns [16]. The transition pruning technique [6] is based on graph theory. This method first builds a transition graph with all possible codewords as nodes and all valid transitions as edges, and then finds a maximum clique. A clique is defined as a subgraph where every pair of nodes are connected with an edge. A maximum clique is defined as a clique of the largest possible size in a given graph. Since every pair of nodes is connected, a maximum clique in this graph

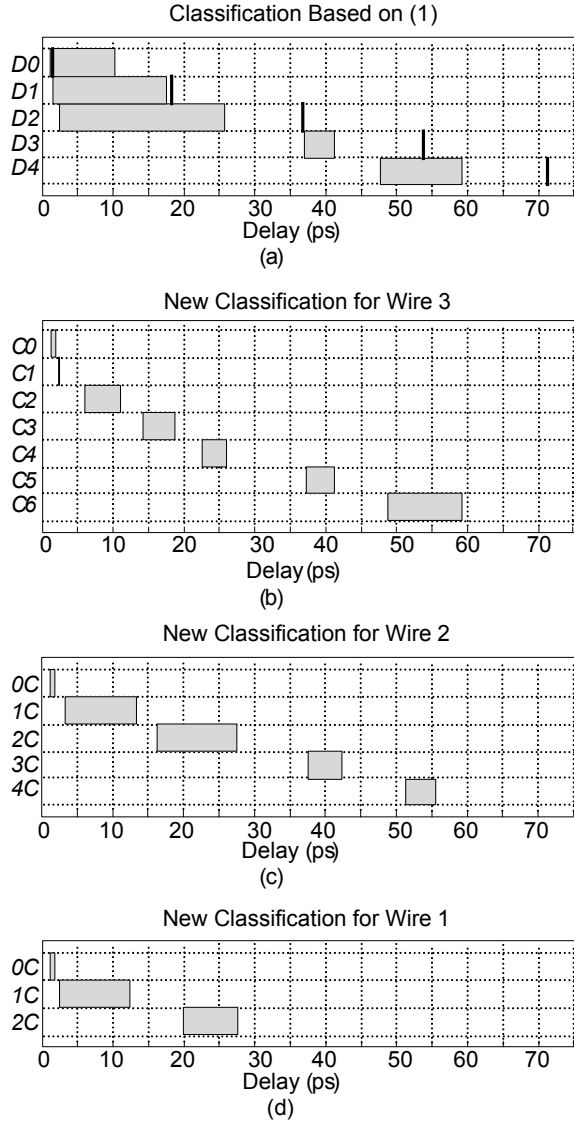


Fig. 4. Simulated delays of different classes of transition patterns using (a) Classification based on (1); (b) Classification with respect to the delay of the middle wire in a five-wire bus; (c) Classification with respect to the delay of wire 2 in a four-wire bus; (d) Classification with respect to the delay of wire 1 in a four-wire bus ( $\lambda = 12.24$  and  $\tau_0 = 1.42$ ps).

constitutes a memoryless codebook with the largest size. The codebook generation method is based on exhaustive search. Although it is easy to get a maximum clique from a transition graph with a small  $n$ , the complexity increases rapidly with  $n$ . This is because the number of edges in an  $n$ -bit transition graph is upper bounded by  $2^{n-1}(2^n - 1)$ , which increases exponentially with  $n$ . In fact, it is an NP problem to find a maximum clique for given constraints [17]. The recursive technique constructs an  $(n + 1)$ -bit codebook from an  $n$ -bit codebook [4], [5]. Since for a small  $n$ , a largest codebook can be obtained easily via the second method, a codebook for an  $n$ -wire bus can be constructed recursively.

### B. CAC Design with New Classification

Since our classification of patterns is different from that in [2], [3], the CAC designs should be reconsidered with our new classification. In the following, we first introduce a recursive

method for codebook construction under different constraints, and then derive the size of codebooks.

In our work, we use the recursive method to obtain a memoryless codebook for the following two reasons. First, it is complex to apply the pattern pruning technique, since our new classification is based on transitions over five wires, and it is not clear which patterns have larger worst-case delays and should be removed. Second, it is hard to find a maximum clique for a transition graph with a large  $n$ . In our method, we first start with a 5-bit codebook, obtained by searching for maximum cliques in a five-wire bus, and then build an  $(n + 1)$ -bit codebook by appending '0' and '1' to codewords of an  $n$ -bit codebook while satisfying delay constraints.

Our new classifications partition patterns over five adjacent wires into seven classes,  $C0$  to  $C6$ , and patterns over four adjacent wires into five classes,  $0C$  to  $4C$ . Similar to the CAC design based on the model in [2], [3], the new classifications are conducive to the design of CACs by eliminating undesirable transition patterns with large worst-case delays.

To get valid 5-bit codebooks, we first assume the allowed patterns are from  $C0$  to  $Ci$  for  $i = 0, 1, \dots, 6$  in our classification for middle wires. Then, for the side wires, we assume patterns are from  $0C$  to  $jC$  based on the classification for side wires. Under these two assumptions, there are many configurations of constraints, which are referred as  $(Ci, jC)$ , where  $i \in \{0, 1, \dots, 6\}$  and  $j \in \{0, 1, \dots, 4\}$ .

Since the worst-case delay of a bus is determined by the largest delays among all wires, for an  $n$ -bit ( $n \geq 5$ ) bus under  $(Ci, jC)$  we require that the worst-case delays on middle wires and side wires are close enough. By our classifications, we find  $0C$  is close to  $C0$ ,  $1C$  close to  $C2$  and  $C3$ ,  $2C$  close to  $C4$ ,  $3C$  close to  $C5$ , and  $4C$  close to  $C6$ . Hence, among all configurations of constraints  $(Ci, jC)$ , we only focus on  $(C0, 0C)$ ,  $(C2, 1C)$ ,  $(C3, 1C)$ ,  $(C4, 2C)$ ,  $(C5, 3C)$ , and  $(C6, 4C)$ . When  $n \leq 4$ , the constraint  $Ci$  cannot be enforced. Hence, the constraint  $(Ci, jC)$  reduces to  $jC$ . The constraint  $(C0, 0C)$  appears to be too restrictive, and hence we do not investigate it in this paper. The last configuration  $(C6, 4C)$  is trivial, since it allows arbitrary transitions.

In the following, we propose a scheme for finding an  $n$ -bit codebook  $C_{(Ci, jC)}(n)$ . For simplicity, we denote  $C_{(Ci, jC)}(n)$  as  $C(n)$  when there is no ambiguity about the constraint. First, for a five-wire bus under constraint  $(Ci, jC)$ , a pattern transition graph is obtained. We search the graph for the largest 5-bit codebooks. One or two 5-bit codebooks of maximum sizes exist for each constraint in Tab. IV, where we denote an  $n$ -bit binary codeword  $(c_1 c_2 \dots c_n)$  as a decimal number  $\sum_{i=1}^n c_i 2^{n-i}$  for simplicity. In [6], a bit boundary in a set of codewords is said to be 01-type if only codewords with 00, 01, and 11 are allowed across that boundary, and a bit boundary is said to be 10-type when only codewords with 00, 10, and 11 are allowed across that boundary. It is shown that the largest clique for a given constraint has alternating boundary types. Thus, there are two largest cliques. Similarly, from Tab. IV, we conjecture that the largest codebooks have alternating constraints,  $C_5^0$  and  $C_5^1$ , for every five consecutive wires. For constraint  $(C4, 2C)$ , only one maximum 5-bit codebook exists. We assume  $C_5^1$  is the same as  $C_5^0$  for constraint  $(C4, 2C)$ .

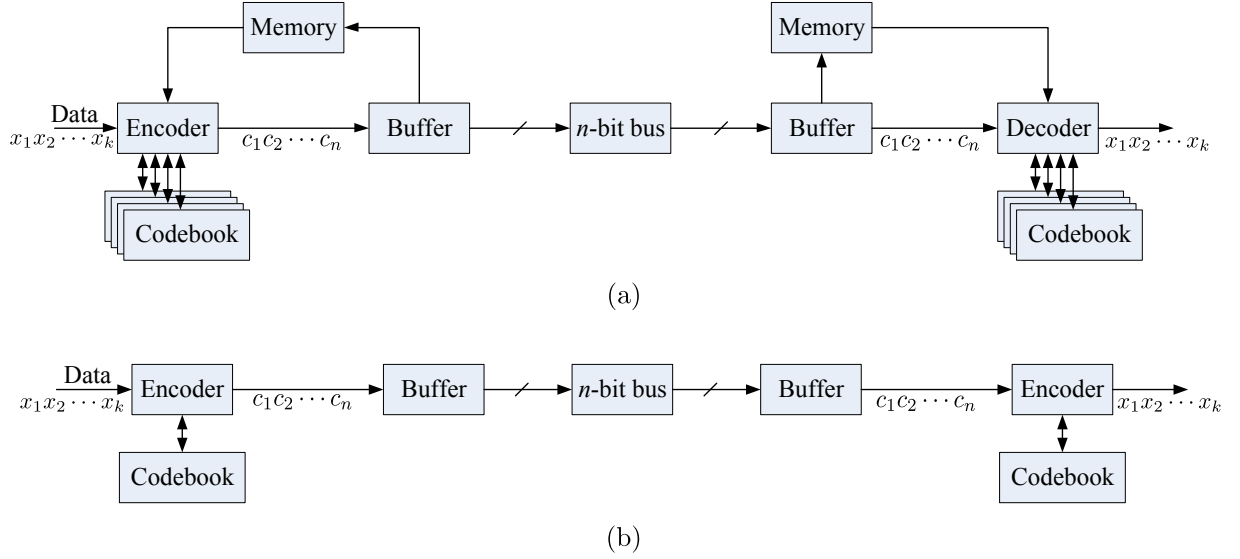


Fig. 5. System model for (a) CACs with memory; (b) Memoryless CACs.

Since we have two types of constraints, two largest codebooks for each constraint can be obtained, except for  $(C4, 2C)$ , where the two codebooks are the same. Then we apply Alg. 1 to obtain  $C(n)$ . In the initialization, we pick a 5-bit codebook  $C_5 = C_5^0$ . Then, the algorithm recursively appends one bit to the codewords in the codebook in each iteration. For  $\mathbf{c}_k = (c_1 c_2 \dots c_k)$ , the appended bit  $x$  needs to satisfy that the last five bits  $(c_{k-3} c_{k-2} c_{k-1} c_k x)$  form a codeword in  $C_5^s$ , which alternates between  $C_5^0$  and  $C_5^1$ . If we pick the other 5-bit codebook  $C_5 = C_5^1$ , we would obtain another codebook.

---

**Algorithm 1** Codebook design under  $(Ci, jC)$

---

**Input:**  $C_5^0, C_5^1, n$ ;

**Initialize:**  $k = 5, C_5 = C_5^0, s = 1$ ;

**while**  $k \leq n - 1$  **do**

**for**  $\forall \mathbf{c}_k = (c_1 c_2 \dots c_k) \in C(k)$  **do**

**if**  $(c_{k-3} c_{k-2} c_{k-1} c_k 0) \in C_5^s$  **then**

      append 0 to  $\mathbf{c}_k$  and add the new codeword to  $C(k+1)$ ;

**else if**  $(c_{k-3} c_{k-2} c_{k-1} c_k 1) \in C_5^s$  **then**

      append 1 to  $\mathbf{c}_k$  and add the new codeword to  $C(k+1)$ ;

**end if**

**end for**

$s = 1 - s$ ;

$k = k + 1$ ;

**end while**

**Output:**  $C(n)$ .

---

The recursive construction allows us to derive the size of the codebooks. Let  $\mathbf{V}_{(Ci, jC)}$  be an all-one  $m$ -dimensional row vector ( $m = |C_5^0|$ ) under constraint  $(Ci, jC)$ . Let  $\mathbf{c}_k^s$  be a  $k$ -bit codeword with last five consecutive bits  $(c_{k-4} c_{k-3} c_{k-2} c_{k-1} c_k) \in C_5^s$  for  $s = 0$  or  $1$ . If a 0 or 1 can be appended to  $\mathbf{c}_k^s$  to form a  $(k+1)$ -bit codeword whose last five bits  $(c_{k-3} c_{k-2} c_{k-1} c_k c_{k+1}) \in C_5^{1-s}$ , such an expansion is called a valid expansion. Otherwise, it is called

an invalid expansion. An expansion matrix is denoted as a  $m \times m$  matrix  $\mathbf{D}_{(Ci, jC)}^s$ , where  $\mathbf{D}_{(Ci, jC)}^s(i, j) = 0$  denotes an invalid expansion and  $\mathbf{D}_{(Ci, jC)}^s(i, j) = 1$  a valid expansion from the  $i$ -th codeword in  $C_5^s$  to the  $j$ -th codeword in  $C_5^{1-s}$  under constraint  $(Ci, jC)$ . Each row of  $\mathbf{D}_{(Ci, jC)}^s$  has at most two ones, since each  $k$ -bit codeword can be appended to form at most two  $(k+1)$ -bit codewords whose last five bits satisfy the appropriate constraints. Let  $\mathbf{Y}$  be an  $m \times m$  anti-diagonal matrix with all ones. Due to symmetry between  $C_5^0$  and  $C_5^1$ ,  $\mathbf{D}^0$  and  $\mathbf{D}^1$  satisfy  $\mathbf{D}_{(Ci, jC)}^1 = \mathbf{Y} \mathbf{D}_{(Ci, jC)}^0 \mathbf{Y}$ . Define  $\mathbf{D}_{(Ci, jC)} = \mathbf{D}_{(Ci, jC)}^0 \mathbf{Y} = \mathbf{Y} \mathbf{D}_{(Ci, jC)}^1$ . We denote  $\mathbf{V}_{(Ci, jC)}$  and  $\mathbf{D}_{(Ci, jC)}$  as  $\mathbf{V}$  and  $\mathbf{D}$ , respectively, when there is no ambiguity about the constraint. Then, for  $n \geq 5$ , the number of codewords in an  $n$ -bit bus is equal to counting the valid transitions and is given by

$$\begin{aligned} |C(n)| &= \mathbf{V} \mathbf{D}^0 \mathbf{D}^1 \dots \mathbf{V}^T \\ &= \begin{cases} \mathbf{V} (\mathbf{D}^0 \mathbf{Y} \mathbf{D}^1)^{\frac{n-5}{2}} \mathbf{V}^T & \text{if } n \text{ is odd;} \\ \mathbf{V} (\mathbf{D}^0 \mathbf{Y} \mathbf{D}^1)^{\frac{n-6}{2}} \mathbf{D}^0 \mathbf{Y} \mathbf{V}^T & \text{if } n \text{ is even;} \end{cases} \\ &= \mathbf{V} \mathbf{D}^{n-5} \mathbf{Y} \mathbf{V}^T. \end{aligned} \quad (6)$$

In the following, we first focus on constraints  $(C3, 1C)$ ,  $(C4, 2C)$ , and  $(C5, 3C)$ . The codes based on these constraints are shown to have the same codebooks as OLCs, FPCs, and FOCs, respectively. Then, we consider constraint  $(C2, 1C)$ , which would lead to codes with a smaller delay at the expense of a lower code rate.

### C. Codes Under $(C3, 1C)$

The one Lambda codes have a worst-case delay  $(1 + \lambda)\tau$ . According to [16], the worst-case delay  $(1 + \lambda)\tau$  can only be achieved **if and only if** the transitions  $\uparrow\downarrow \times$ ,  $\uparrow\downarrow -$ , and  $\uparrow\downarrow \uparrow$  plus their symmetric and complement versions (e.g.  $\uparrow\downarrow \times$  and  $\times \downarrow\uparrow$  are symmetric, and  $\downarrow\downarrow -$  is the complement of  $\downarrow\downarrow \uparrow$ ) are avoided, where  $\uparrow$ ,  $\downarrow$ ,  $\times$ , and  $-$  denote  $0 \rightarrow 1$ ,  $1 \rightarrow 0$ , don't care, and no transition, respectively. The first constraint of avoiding  $\uparrow\downarrow \times$  ensures that a transition between any two



TABLE IV  
LARGEST 5-BIT CODEBOOK(S) UNDER CONSTRAINT  $(Ci, jC)$ .

Constraint	$C_5^0$	$C_5^1$
$(C5, 3C)$	$\{0, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 24, 25, 26, 27, 28, 30, 31\}$	$\{0, 1, 3, 4, 5, 6, 7, 12, 13, 14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31\}$
$(C4, 2C)$	$\{0, 1, 3, 6, 7, 12, 14, 15, 16, 17, 19, 24, 25, 28, 30, 31\}$	
$(C3, 1C)$	$\{0, 3, 14, 15, 24, 30, 31\}$	$\{0, 1, 7, 16, 17, 28, 31\}$
$(C2, 1C)$	$\{0, 3, 15, 24, 30, 31\}$	$\{0, 1, 7, 16, 28, 31\}$

TABLE V  
EXPANSION MATRIX FOR  $(C3, 1C)$ ,  $(C4, 2C)$ , AND  $(C5, 3C)$ .

[illegible]

codewords does not cause opposite transition on any wire. This condition is referred as a forbidden-transition (FT) condition. The second constraint of avoiding  $-\uparrow$ - ensures that 2C patterns are removed. This constraint ensures two adjacent bit boundaries cannot both be 01-type or 10-type, and is referred as a forbidden adjacent boundary pattern (FABP) condition [16]. The last two forbidden patterns give the constraint that no patterns 010 and 101 appear in the codeword, which is referred as a forbidden-pattern (FP) condition [16]. Codes satisfying these **necessary and sufficient** conditions are called one Lambda codes (OLCs). We denote the largest OLC codebook size for an  $n$ -bit bus as  $G_n$ , and  $G_n$  is given by

$$G_n = G_{n-1} + G_{n-5} \quad (7)$$

with initial conditions  $G_1 = 2, G_2 = 3, G_3 = 4, G_4 = 5$ , and  $G_5 = 7$  [18].

With our classification, we explore codes under constraint  $(C3, 1C)$ . From Tab. IV, the two largest 5-bit codebooks are given by  $C_5^0=\{0, 3, 14, 15, 24, 30, 31\}$  and  $C_5^1=\{0, 1, 7, 16, 17, 28, 31\}$ . An  $n$ -bit codebook  $C(n)$  can be obtained via Alg. 1. The number of codewords is given by

$$|C(n)| = \mathbf{V} \mathbf{D}_{(C3,1C)}^{n-5} \mathbf{V}^T \text{ for } n \geq 5, \quad (8)$$

where  $\mathbf{V}$  is a seven-dimensional all one vector and  $\mathbf{D}_{(C3,1C)}$  is a  $7 \times 7$  expansion matrix as shown in Tab. V. We further establish that the largest codebook sizes under constraint  $(C3, 1C)$  satisfy the recursion:

**Lemma III.1.** For  $n \geq 8$ ,  $|C_{(C3,1C)}(n)|$  is given by a recursion  $|C_{(C3,1C)}(n)| = |C_{(C3,1C)}(n-2)| + |C_{(C3,1C)}(n-3)|$ , with initial conditions  $|C_{(C3,1C)}(n)| = 7, 9, 12$ , for  $n = 5, 6, 7$ , respectively.

See the appendix for the proof. In fact, we can further relate these codes with OLCs by the following:

**Theorem III.1.** *The codes under  $(C3, 1C)$  have the same codebooks as OLCs. Hence,  $G_n = |C_{(C3, 1C)}(n)|$ .*

See the appendix for the proof. Theorem III.1 implies that the codes under constraint  $(C3, 1C)$  are equivalent to the class of OLC codes.

#### D. Codes Under $(C4, 2C)$

The  $(1 + 2\lambda)$  codes have a worst-case delay of  $(1 + 2\lambda)\tau$ . No necessary and sufficient condition is known for a code to be a  $(1 + 2\lambda)$  code. Two sufficient conditions FT and FP are found, which lead to two families of  $(1 + 2\lambda)$  codes, FTC and FPC, respectively. The size of an FTC codebook for an  $n$ -wire bus is given by  $F_{n+2}$ , where  $F_n$  is the Fibonacci sequence that satisfies  $F_{n+2} = F_{n+1} + F_n$  and has initial conditions  $F_1 = F_2 = 1$  [6]. The FPCs for an  $n$ -wire bus have a larger codebook size  $2F_{n+1}$  [4].

With our classification, we explore codes under constraint  $(C4, 2C)$ . From Tab. IV, only one largest 5-bit codebook is found  $C_5^0 = \{0, 1, 3, 6, 7, 12, 14, 15, 16, 17, 19, 24, 25, 28, 30, 31\}$ . An  $n$ -bit codebook  $C(n)$  can be obtained via Alg. 1 by setting  $C_5^1 = C_5^0$ . The number of codewords is given by

$$|C(n)| = \mathbf{V} \mathbf{D}_{(C4,2C)}^{n-5} \mathbf{V}^T \text{ for } n \geq 5 \quad (9)$$

where  $\mathbf{V}$  is a 16-dimensional all one vector and  $\mathbf{D}_{(C4,2C)}$  is a  $16 \times 16$  expansion matrix as shown in Tab. V. We further establish that the largest codebook sizes under constraint  $(C4, 2C)$  satisfy the recursion:

**Lemma III.2.** For  $n \geq 9$ ,  $|C_{(C4,2C)}(n)|$  can be simplified as recursion  $|C_{(C4,2C)}(n)| = 2|C_{(C4,2C)}(n-1)| -$

$|C_{(C4,2C)}(n-2)| + |C_{(C4,2C)}(n-4)|$ , with boundary conditions  $|C_{(C4,2C)}(n)| = 16, 26, 42, 68$ , for  $n = 5, 6, 7, 8$ , respectively.

See the appendix for the proof. Again, we can relate these codes to existing CACs by the following:

**Theorem III.2.** *The codes under  $(C4, 2C)$  have the same codebooks as FPCs. Hence,  $2F_{n+1} = |C_{(C4,2C)}(n)|$ .*

See the appendix for the proof. Since FPCs and our codes under  $(C4, 2C)$  can be obtained by excluding  $D3$  plus  $D4$  patterns and  $C5$  plus  $C6$  patterns, respectively, Theorem III.2 is not surprising given that  $C5$  and  $C6$  are the same as  $D3$  and  $D4$ , respectively. Theorem III.2 implies that results in the literature regarding FPCs are also applicable to codes under constraint  $(C4, 2C)$ .

#### E. Codes Under $(C5, 3C)$

The  $(1 + 3\lambda)$  codes have a worst-case delay of  $(1 + 3\lambda)\tau$ , which can be achieved **if and only if**  $\downarrow\uparrow\downarrow$  and  $\uparrow\downarrow\uparrow$  are avoided. So the **necessary and sufficient** condition for the  $(1 + 3\lambda)$  codes is that the codebook cannot have both 010 and 101 appearing centered around any bit position, which is referred as a forbidden-overlap (FO) condition. Codes satisfying the FO condition are called FOCs. It is shown that the largest FOC codebook for an  $n$ -bit bus is given by  $T_{n+2}$ , where  $T_n = T_{n-1} + T_{n-2} + T_{n-3}$  is the tribonacci number sequence with initial conditions  $T_1 = 1, T_2 = 1$ , and  $T_3 = 2$  [16].

With our classification, we explore codes under constraint  $(C5, 3C)$ . Two largest 5-bit codebooks  $C_5^0 = \{0, 1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 24, 25, 26, 27, 28, 30, 31\}$  and  $C_5^1 = \{0, 1, 3, 4, 5, 6, 7, 12, 13, 14, 15, 16, 17, 19, 20, 21, 22, 23, 24, 25, 28, 29, 30, 31\}$  are found. Via Alg. 1, an  $n$ -bit codebook  $C(n)$  can be obtained. The number of codewords is given by

$$|C(n)| = \mathbf{V}\mathbf{D}_{(C5,3C)}^{n-5}\mathbf{V}^T \text{ for } n \geq 5, \quad (10)$$

where  $\mathbf{V}$  is a 24-dimensional all one vector and  $\mathbf{D}_{(C5,3C)}$  is a  $24 \times 24$  expansion matrix as shown in Tab. V.

We further establish that the largest codebook sizes under constraint  $(C5, 3C)$  satisfy the recursion:

**Lemma III.3.** *For  $n \geq 8$ ,  $|C_{(C5,3C)}(n)|$  can be simplified as recursion  $|C_{(C5,3C)}(n)| = |C_{(C5,3C)}(n-1)| - |C_{(C5,3C)}(n-2)| + |C_{(C5,3C)}(n-3)|$ , with boundary conditions  $|C_{(C5,3C)}(n)| = 24, 44, 81$ , for  $n = 5, 6, 7$ , respectively.*

See the appendix for the proof. Again we can relate these codes to existing CACs by the following:

**Theorem III.3.** *The codes under  $(C5, 3C)$  have the same codebooks as FOCs. Hence,  $T_{n+2} = |C_{(C5,3C)}(n)|$ .*

See the appendix for the proof. Theorem III.3 is not surprising, since FOCs and our codes under  $(C5, 3C)$  can be obtained by excluding  $D4$  and  $C6$  patterns, respectively, and  $D4$  and  $C6$  have been shown to be the same. Theorem III.3 implies that results in the literature regarding FOCs are also applicable to codes under constraint  $(C5, 3C)$ .

#### F. Codes Under $(C2, 1C)$

With our classification, we explore codes under constraint  $(C2, 1C)$ . From Tab. IV, the two largest 5-bit codebooks are given by  $C_5^0 = \{00000, 00011, 01111, 11000, 11110, 11111\}$  and  $C_5^1 = \{00000, 00001, 00111, 10000, 11100, 11111\}$ . An  $n$ -bit codebook  $C(n)$  can be obtained via Alg. 1. The number of codewords is given by

$$|C(n)| = \mathbf{V}\mathbf{D}^{n-5}\mathbf{V}^T \text{ for } n \geq 5, \quad (11)$$

where  $\mathbf{V}$  is a six-dimensional all one vector and  $\mathbf{D} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ .

We further establish that the largest codebook sizes under constraint  $(C2, 1C)$  satisfy the recursion:

**Lemma III.4.** *For  $n \geq 10$ ,  $|C_{(C2,1C)}(n)|$  can be simplified as recursion  $|C_{(C2,1C)}(n)| = |C_{(C2,1C)}(n-2)| + |C_{(C2,1C)}(n-5)|$ , with initial conditions  $|C_{(C2,1C)}(n)| = 6, 7, 9, 11, 14$ , for  $n = 5, 6, 7, 8, 9$ , respectively.*

See the appendix for the proof.

**Lemma III.5.** *The codebook under  $(C2, 1C)$  is a subset of OLC.*

See the appendix for the proof.

#### G. Pruned Codes Under $(C2, 1C)$

For  $(C2, 1C)$ , the restriction on the side wires is more relaxed than that on the middle wires, which results in larger worst-case delays for the side wires. Hence, we prune the CACs under constraint  $(C2, 1C)$  by removing codewords with larger delays on the side wires in order to achieve a smaller worst-case delay. Since the pruned codes have a smaller delay than OLCs, we call these pruned CACs improved one Lambda codes (IOLCs). We obtain IOLCs by first finding an  $n$ -bit codebook via Alg. 1 as in Sec. III-F, and then pruning the codebook with Alg. 2. To prune the codebook  $C(n)$ , we search for maximum subsets of  $C_5^i$  ( $i = 0, 1$ ) with smaller delays on the side wires. For  $C_5^0$ , two maximum subsets  $C_5^{0,0} = \{0, 3, 15, 30, 31\}$  and  $C_5^{0,1} = \{0, 15, 24, 30, 31\}$  are found with smaller worst-case delays on wires 1 and 2 and wires 4 and 5, respectively. For  $C_5^1$ , a maximum subset  $C_5^{1,1} = \{0, 1, 7, 16, 31\}$  is found with smaller worst-case delays on wires 4 and 5. Finally, a valid  $n$ -bit codebook is obtained with the leftmost five bits belonging to  $C_5^{0,0}$ , and the rightmost five bits belonging to  $C_5^{0,1}$  or  $C_5^{1,1}$  depending on whether  $n$  is odd or even.

The pruning algorithm for CACs under  $(C2, 1C)$  on an  $n$ -bit bus is shown in Alg. 2. By pruning all codewords  $c_n$  in  $C(n)$ , the algorithm removes codewords with larger delay on side wires. With Alg. 2, we get an  $n$ -bit IOLC under constraint  $(C2, 1C)$ , and its size is given by

$$|C_{IOLC}(n)| = \mathbf{W}_1\mathbf{D}^{n-5}\mathbf{W}_2^T \text{ for } n \geq 5, \quad (12)$$

where  $\mathbf{W}_1 = [1 \ 1 \ 1 \ 0 \ 1 \ 1]$ ,  $\mathbf{W}_2 = [1 \ 0 \ 1 \ 1 \ 1 \ 1]$ , and  $\mathbf{D}$  is the same as that in Eq. (11). Note that  $\mathbf{W}_1$  and  $\mathbf{W}_2$  are used instead of  $\mathbf{V}$ , because of the pruning of valid patterns on side wires.

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**Algorithm 2** Pruning CACs under  $(C2, 1C)$ 


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**Input:**  $C_5^{0,0}$ ,  $C_5^{0,1}$ ,  $C_5^{1,1}$ ,  $C(n)$ ;  
**if**  $n$  is odd **then**  
     $i = 1$ ;  
**else**  
     $i = 0$ ;  
**end if**  
**for**  $\forall c_n = (c_1 c_2 \dots c_n) \in C(n)$  **do**  
    **if**  $(c_1 c_2 c_3 c_4 c_5) \notin C_5^{0,0}$  **or**  $(c_{n-4} c_{n-3} c_{n-2} c_{n-1} c_n) \notin C_5^{1-i,1}$  **then**  
        eliminate  $c_n$  from  $C(n)$ ;  
    **end if**  
**end for**  
**Output:**  $C(n)$ .

---

We further establish that the largest codebook sizes of IOLCs satisfy the recursion:

**Lemma III.6.** For  $n \geq 10$ ,  $|C_{IOLC}(n)|$  can be simplified as recursion  $|C_{IOLC}(n)| = |C_{IOLC}(n-2)| + |C_{IOLC}(n-5)|$ , with initial conditions  $|C_{IOLC}(n)| = 4, 5, 7, 8, 11$ , for  $n = 5, 6, 7, 8, 9$ , respectively.

This recursion is the same as that in that in Lemma III.4. It can be proved in the same fashion as for Lemma III.4, and hence its proof is omitted.

**Lemma III.7.** The IOLC codebook is a subset of OLC.

See the appendix for the proof.

TABLE VI

SIMULATED DELAYS OF OUR IOLC, UNPRUNED  $(C2, 1C)$  CODE, AND OLC [5] FOR A 10-BIT BUS ( $\lambda = 12.24$  AND  $\tau_0 = 1.42$ ps).

Wire $i$	Delays (ps)		
	IOLCs	$(C2, 1C)$	OLCs
1	10.08	5.49	10.55
2	7.03	9.13	2.92
3	9.31	9.31	5.94
4	9.31	9.45	6.09
5	9.59	9.36	10.73
6	9.41	9.41	13.64
7	<b>10.14</b>	10.14	14.06
8	9.65	10.57	14.84
9	8.97	9.14	8.99
10	5.28	<b>13.50</b>	<b>14.84</b>

#### IV. PERFORMANCE EVALUATION

In this section, we evaluate the performance of CACs based on our classification with extensive simulations, and compare them with existing CACs. Each CAC has two key performance metrics: delay and rate. The delay of a CAC is the worst-case delay when the codewords from the CAC are transmitted over the bus. Codebook size and code rate are often used to measure the overhead of CACs. The codebook size of a CAC is simply the number of codewords. Suppose a CAC of size  $M$  is transmitted over an  $n$ -bit bus, then its rate is defined as  $\frac{\log_2 M}{n}$ . A CAC of rate  $k/n$  implies that  $n - k$  extra wires are used in addition to  $k$  data wires so as to reduce the crosstalk delay. Hence, the code rate measures the area and

TABLE VII

SIMULATED DELAYS OF OUR IOLC, UNPRUNED  $(C2, 1C)$  CODE, AND OLC [5] FOR A 16-BIT BUS ( $\lambda = 12.24$  AND  $\tau_0 = 1.42$ ps).

Wire $i$	Delays (ps)		
	IOLCs	$(C2, 1C)$	OLCs
1	10.32	<b>13.92</b>	15.95
2	7.43	9.51	10.03
3	9.57	10.88	15.54
4	9.83	10.21	15.75
5	10.16	10.16	15.02
6	10.33	10.34	15.57
7	10.39	10.39	15.70
8	10.23	10.23	15.48
9	9.87	10.25	15.57
10	<b>10.40</b>	10.39	15.66
11	10.34	10.33	15.52
12	10.17	10.21	14.88
13	10.25	10.39	15.85
14	9.98	10.92	15.59
15	9.61	9.62	10.13
16	5.58	13.92	<b>16.11</b>

power overhead of CACs: the higher the rate, the smaller the overhead. Obviously, there is a tradeoff between the code rate and delay of a CAC: typically a lower rate code is needed to achieve a smaller delay. To measure the overall effects of both rate and delay, we also define the throughput of a CAC as the ratio of code rate and delay. The assumptions for this definition are: (1) the clock rate of the bus is determined by the inverse of the worst-case delay; (2) the throughput of the bus is linearly proportional to  $k$ , the number of data wires.

Since codes under  $(C3, 1C)$ ,  $(C4, 2C)$ , and  $(C5, 3C)$  have exactly the same codebooks as OLCs, FPCs, and FOCs, their delay, rate, and throughput are also the same. Under constraint  $(C2, 1C)$ , we propose two kinds of codes, unpruned codes and pruned codes (IOLCs). In the following, we compare their performance with OLCs in [5] with extensive simulations.

To compare the worst-case delay of our IOLCs, unpruned  $(C2, 1C)$  codes, and OLCs, we simulate two buses, a 10-bit bus and a 16-bit bus, with all transitions between any two codewords in their codebooks and obtain the worst-case delays of each wire. The simulation environment has been explained in Sec. II-C. Both buses have a length of 5mm, and  $\tau_0 = 1.42$ ps and  $\lambda = 12.24$ . The simulation results are shown in Tabs. VI and VII, where for each CAC the largest delays among all wires are in boldface. As commented above for unpruned  $(C2, 1C)$  codes, the delays of the two outmost wires are significantly greater than those of other wires. For a 10-bit bus, the worst-case delays of our IOLC, unpruned  $(C2, 1C)$  code, and an OLC are given by 10.14ps, 13.50ps, and 14.84ps, respectively. The worst-case delay of our IOLC and unpruned  $(C2, 1C)$  code are 31.67% and 9.03% smaller than that of the OLC, respectively. For a 16-bit bus, the worst-case delays of our IOLC, unpruned  $(C2, 1C)$  code, and an OLC are given by 10.40ps, 13.92ps, and 16.11ps, respectively. The worst-case delay of our IOLC and unpruned  $(C2, 1C)$  code are 35.44% and 13.59% smaller than that of the OLC, respectively.

For all simulations, our IOLCs have better delay performance than OLCs. Although both IOLCs and unpruned  $(C2, 1C)$  codes have almost the same code rate and better

TABLE VIII  
COMPARISON OF CODEBOOK SIZE AND THROUGHPUT OF IOLC, UNPRUNED ( $C2, 1C$ ) CODE, AND OLC [5] ( $\lambda = 12.24$  AND  $\tau_0 = 1.42\text{ps}$ ).

# of wires	IOLC			$(C2, 1C)$			OLC	
	# of words	# of bits	Throughput Gain	# of words	# of bits	Throughput Gain	# of words	# of bits
5	4	2	<b>1.55</b>	6	2	<b>1.10</b>	7	2
6	5	2	1.07	7	2	0.78	9	3
7	7	2	1.02	9	3	1.14	12	3
8	8	3	1.12	11	3	0.84	16	4
9	11	3	1.10	14	3	0.84	21	4
10	12	3	1.10	17	4	<b>1.10</b>	28	4
11	16	4	1.18	21	4	0.88	37	5
12	18	4	1.19	26	4	0.89	49	5
13	23	4	1.03	32	5	0.96	65	6
14	27	4	1.02	40	5	0.95	86	6
15	34	5	1.27	49	5	0.95	114	6
16	41	5	1.11	61	5	0.83	151	7

delay performance than OLCs, the delay performance of IOLCs is much better than the unpruned ( $C2, 1C$ ) codes. With a more advanced technology where the coupling effect is significant, the improvement of our IOLCs is bigger.

The comparisons of the codebook size between our IOLCs, unpruned ( $C2, 1C$ ) codes, and OLCs [5] and the throughput gain with respect to OLCs are shown in Tab. VIII. The throughput gain of our CACs with respect to OLCs is given by the ratio between the throughput of our CACs and the throughput of OLCs. The codebook sizes of the three codes are close. In all cases, the difference of the number of bits between our IOLCs and unpruned ( $C2, 1C$ ) codes is within 1 bit. The difference of the number of bits between our IOLCs and OLCs [5] is within 2 bits for  $n \leq 16$ . In respect to throughput, our IOLCs always have a greater throughput than OLCs, and their throughput gain ranges from 1.02 to 1.55 for an  $n$ -wire bus ( $5 \leq n \leq 16$ ). The unpruned ( $C2, 1C$ ) codes have better throughput in some cases than OLCs, and the throughput gain ranges from 0.78 to 1.10 for an  $n$ -wire bus ( $5 \leq n \leq 16$ ). When unpruned ( $C2, 1C$ ) codes have a lower throughput than OLCs, IOLCs can be used.

Our IOLCs and unpruned ( $C2, 1C$ ) codes provide additional options for the tradeoff between code rate and code delay. In addition to achieving higher throughputs, the new CACs are also appropriate for interconnects where the delay is of top priority.

It has been shown that the encoding and decoding of OLCs, FPCs, and FOCs have quadratic complexity based on numeral systems [11]. Since codes under ( $C3, 1C$ ), ( $C4, 2C$ ), and ( $C5, 3C$ ) have exactly the same codebooks as OLCs, FPCs, and FOCs, their CODECs also have quadratic complexity. Also, it is expected that the encoding and decoding of our IOLCs and unpruned ( $C2, 1C$ ) codes have a quadratic complexity, since the codebooks of our IOLCs and unpruned ( $C2, 1C$ ) codes are proper subsets of OLCs.

We remark that the simulation results in Sections II-C and IV are all based on a 45nm CMOS technology. We have also run the same set of simulations based on a 0.1- $\mu\text{m}$  technology (omitted for brevity). Between the two sets of simulation results, the main conclusions of the manuscript and the key features of our proposed classification and CACs remain the same. For instance, the delays of the patterns in different classes do not overlap, regardless of the technology. Also, the

proposed CACs based on the new classification are also the same. This actually demonstrates that our approach to delay classification and CACs is applicable to a wide variety of technology. This is because in our approach, the dependency of the crosstalk delay on the technology is represented by the two parameters, the propagation delay  $\tau_0$  of a wire free of crosstalk and the coupling factor  $\lambda$ . Since our analytical approach to the classification and CACs treats these two parameters as variables, our approach can be easily adapted to a wide variety of technology.

## V. CONCLUSIONS

In this paper, we propose a new classification of transition patterns. The new classification has finer classes and the delays do not overlap among different classes. Hence the new classification is conducive to the design of CACs. To illustrate this, we design a family of CACs with different constraints. Some codes of the family are the same as existing codes, OLCs, FPCs, and FOCs. We also propose two new CACs with a smaller worst-case delay and better throughput than OLCs. Since our analytical approach to the classification and CACs treats the technology-dependent parameters as variables, our approach can be easily adapted to a wide variety of technology.

## APPENDIX

*Proof of Lemma III.1:* The eigenvalues of  $\mathbf{D}$  are given by solving  $\det|\lambda\mathbf{I} - \mathbf{D}| = 0$ . Then,

$$\begin{aligned}
 & \det|\lambda\mathbf{I} - \mathbf{D}| = 0 \\
 \Rightarrow & \lambda^7 - \lambda^5 - \lambda^4 = 0 \\
 \Rightarrow & \mathbf{D}^7 = \mathbf{D}^5 + \mathbf{D}^4 \\
 \Rightarrow & \mathbf{V}\mathbf{D}^7\mathbf{V}^T = \mathbf{V}\mathbf{D}^5\mathbf{V}^T + \mathbf{V}\mathbf{D}^4\mathbf{V}^T \\
 \Rightarrow & |C(n)| = |C(n-2)| + |C(n-3)|.
 \end{aligned}$$

For  $n = 5, 6, 7$ , the boundary conditions can be obtained by Eq. (8) as  $|C(5)| = 7$ ,  $|C(6)| = 9$ , and  $|C(7)| = 12$ . Thus, the lemma holds for  $n \geq 8$ . ■

*Proof of Theorem III.1:* It has been shown that an  $(n+1)$ -bit OLC codebook  $C(n+1)$  can be constructed from an  $n$ -bit codebook  $C(n)$  [5]. The necessary and sufficient condition for OLCs defines the same expansion matrix as our codes. The OLC construction is the same as that of our codes under ( $C3, 1C$ ) shown in Alg. 1. For  $n = 5$ , the OLC codebooks

are the same as our codes under  $(C3, 1C)$ . So, for an  $n$ -bit bus ( $n \geq 5$ ), codes under constraint  $(C3, 1C)$  are the same as OLCs. For an  $n$ -bit bus ( $n \leq 4$ ), the constraint  $(C3, 1C)$  reduces to  $1C$ , and leads to the same codebooks as OLCs. Hence, our codes under  $(C3, 1C)$  have the same codebooks as OLCs, which implies that  $G_n = |C(n)|$ . ■

*Proof of Lemma III.2:* The eigenvalues of  $\mathbf{D}$  are given by solving  $\det |\lambda \mathbf{I} - \mathbf{D}| = 0$ . Then,

$$\begin{aligned} \det |\lambda \mathbf{I} - \mathbf{D}| &= 0 \\ \Rightarrow \mathbf{D}^{16} &= 2\mathbf{D}^{15} - \mathbf{D}^{14} + \mathbf{D}^{12} \\ \Rightarrow \mathbf{V}\mathbf{D}^{16}\mathbf{V}^T &= 2\mathbf{V}\mathbf{D}^{15}\mathbf{V}^T - \mathbf{V}\mathbf{D}^{14}\mathbf{V}^T + \mathbf{V}\mathbf{D}^{12}\mathbf{V}^T \\ \Rightarrow |C(n)| &= 2|C(n-1)| - |C(n-2)| + |C(n-4)|. \end{aligned}$$

For  $n = 5, 6, 7, 8$ , the boundary conditions can be obtained by Eq. (9) as  $|C(5)| = 16$ ,  $|C(6)| = 26$ ,  $|C(7)| = 42$ , and  $|C(8)| = 68$ . Thus, the lemma holds for  $n \geq 9$ . ■

*Proof of Theorem III.2:* It has been shown that an  $(n+1)$ -bit FPC codebook  $C(n+1)$  can be constructed from an  $n$ -bit codebook  $C(n)$  [4]. The sufficient condition (FP condition) for FPCs defines the same expansion matrix as our codes. The FPC construction is the same as that of our codes under  $(C4, 2C)$  shown in Alg. 1. For  $n = 5$ , the FPC codebooks are the same as our codes under  $(C4, 2C)$ . So, for an  $n$ -bit bus ( $n \geq 5$ ), codes under constraint  $(C4, 2C)$  are the same as FPCs. For an  $n$ -bit bus ( $n \leq 4$ ), the constraint  $(C4, 2C)$  reduces to  $2C$ , and leads to the same codebooks as FPCs. Hence, our codes under  $(C4, 2C)$  have the same codebooks as FPCs, which implies that  $2F_{n+1} = |C(n)|$ . ■

*Proof of Lemma III.3:* The eigenvalues of  $\mathbf{D}$  are given by solving  $\det |\lambda \mathbf{I} - \mathbf{D}| = 0$ . Then,

$$\begin{aligned} \det |\lambda \mathbf{I} - \mathbf{D}| &= 0 \\ \Rightarrow \mathbf{D}^{24} &= \mathbf{D}^{23} + \mathbf{D}^{22} + \mathbf{D}^{21} \\ \Rightarrow \mathbf{V}\mathbf{D}^{24}\mathbf{V}^T &= \mathbf{V}\mathbf{D}^{23}\mathbf{V}^T + \mathbf{V}\mathbf{D}^{22}\mathbf{V}^T + \mathbf{V}\mathbf{D}^{21}\mathbf{V}^T \\ \Rightarrow |C(n)| &= |C(n-1)| + |C(n-2)| + |C(n-3)|. \end{aligned}$$

For  $n = 5, 6, 7, 8$ , the boundary conditions can be obtained by Eq. (10) as  $|C(5)| = 24$ ,  $|C(6)| = 44$ , and  $|C(7)| = 81$ . Thus, the lemma holds for  $n \geq 9$ . ■

*Proof of Theorem III.3:* It has been shown that an  $(n+1)$ -bit FOC codebook  $C(n+1)$  can be constructed from an  $n$ -bit codebook  $C(n)$  [4]. The necessary and sufficient condition (FO condition) for FOCs defines the same expansion matrix as our codes. The FOC construction is the same as that of our codes under  $(C5, 3C)$  shown in Alg. 1. For  $n = 5$ , the FOC codebooks are the same as our codes under  $(C5, 3C)$ . So, for an  $n$ -bit bus ( $n \geq 5$ ), codes under constraint  $(C5, 3C)$  are the same as FOCs. For an  $n$ -bit bus ( $n \leq 4$ ), the constraint  $(C5, 3C)$  reduces to  $3C$ , and leads to the same codebooks as FOCs. Hence, our codes under  $(C5, 3C)$  have the same codebooks as FOCs, which implies that  $T_{n+2} = |C(n)|$ . ■

*Proof of Lemma III.4:* The eigenvalues of  $\mathbf{D}$  are given by solving  $\det |\lambda \mathbf{I} - \mathbf{D}| = 0$ . Then,

$$\begin{aligned} \det |\lambda \mathbf{I} - \mathbf{D}| &= 0 \\ \Rightarrow \mathbf{D}^6 &= \mathbf{D}^4 - \mathbf{D} \\ \Rightarrow \mathbf{V}\mathbf{D}^6\mathbf{V}^T &= \mathbf{V}\mathbf{D}^4\mathbf{V}^T + \mathbf{V}\mathbf{D}\mathbf{V}^T \\ \Rightarrow |C(n)| &= |C(n-2)| + |C(n-5)|. \end{aligned}$$

For  $n = 5, 6, 7, 8, 9$ , the boundary conditions can be obtained by Eq. (11) as  $|C(5)| = 6$ ,  $|C(6)| = 7$ ,  $|C(7)| = 9$ ,  $|C(8)| = 11$ , and  $|C(9)| = 14$ . Thus, the lemma holds for  $n \geq 10$ . ■

*Proof of Lemma III.5:* As shown in Tab. IV,  $C_5^i$  under  $(C2, 1C)$  is a subset of  $C_5^i$  under  $(C3, 1C)$  for  $i = 0, 1$ . Thus, the valid expansions from  $C_5^i$  to  $C_5^{1-i}$  under  $(C2, 1C)$  is part of that under  $(C3, 1C)$ . So, for an  $n$ -bit bus,  $C_{(C2, 1C)}(n) \subset C_{(C3, 1C)}(n)$ . According to Thm. III.1, the  $n$ -bit codebook  $C_{(C2, 1C)}(n)$  is a subset of an OLC codebook. ■

*Proof of Lemma III.7:* Since the IOLC codebook is a subset of the unpruned codes under  $(C2, 1C)$ , this follows Lemma III.5. ■

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